

Electronic Protection Array for ESD and Over-Voltage Protection

The SP721 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

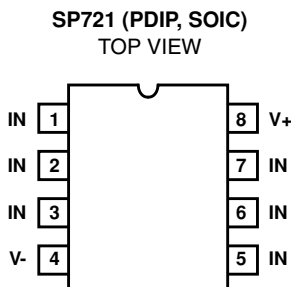
HBM STANDARD	MODE	R	C	ESD (V)
IEC 1000-4-2	Air	330Ω	150pF	>15kV
	Direct	330Ω	150pF	>4kV
	Direct, Dual Pins	330Ω	150pF	>8kV
MIL-STD-3015.7	Direct, In-Circuit	1.5kΩ	100pF	>15kV

Refer to Figure 1 and Table 1 for further detail. Refer to Application Notes AN9304 and AN9612 for additional information.

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
SP721AP	-40 to 105	8 Ld PDIP	E8.3
SP721AB	-40 to 105	8 Ld SOIC	M8.15
SP721ABT	-40 to 105	8 Ld SOIC Tape and Reel	M8.15

Pinout



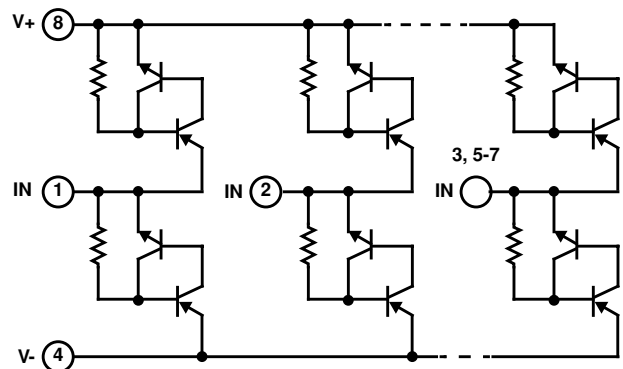
Features

- ESD Interface Capability for HBM Standards
 - MIL STD 3015.7 15kV
 - IEC 1000-4-2, Direct Discharge,
 - Single Input 4kV (Level 2)
 - Two Inputs in Parallel 8kV (Level 4)
 - IEC 1000-4-2, Air Discharge 15kV (Level 4)
- High Peak Current Capability
 - IEC 1000-4-5 (8/20μs) ±3A
 - Single Pulse, 100μs Pulse Width ±2A
 - Single Pulse, 4μs Pulse Width ±5A
- Designed to Provide Over-Voltage Protection
 - Single-Ended Voltage Range to +30V
 - Differential Voltage Range to ±15V
- Fast Switching 2ns Rise Time
- Low Input Leakages 1nA at 25°C Typical
- Low Input Capacitance 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Functional Block Diagram



Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-) +35V
 Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND
 (Refer to Figure 6) ±2A, 100µs
 ESD Ratings and Capability (Figure 1, Table 1)
 Load Dump and Reverse Battery (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
 PDIP Package 160
 SOIC Package 170
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC}, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V _{SUPPLY} = [(V+) - (V-)]	V _{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop IN to V- IN to V+	V _{FWDL} V _{FWDH}	I _{IN} = 1A (Peak Pulse)	- -	2 2	- -	V V
Input Leakage Current	I _{IN}		-20	5	+20	nA
Quiescent Supply Current	I _{QUIESCENT}		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V _{FWD} /I _{FWD} ; Note 3	-	1	-	Ω
Input Capacitance	C _{IN}		-	3	-	pF
Input Switching Speed	t _{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP721 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 1000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R _D	C _D	±V _D
MIL-STD-3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 1000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

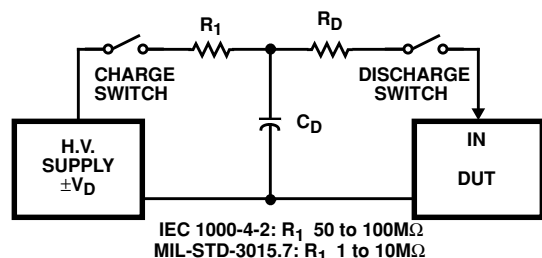


FIGURE 1. ELECTROSTATIC DISCHARGE TEST

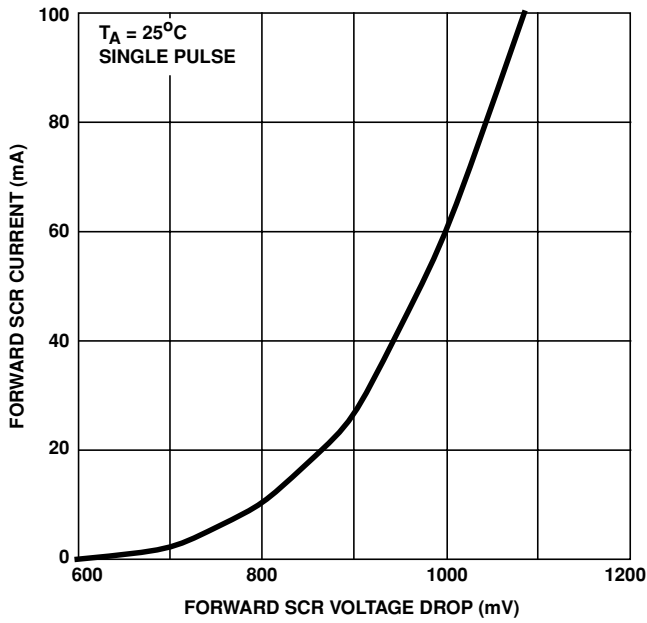


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

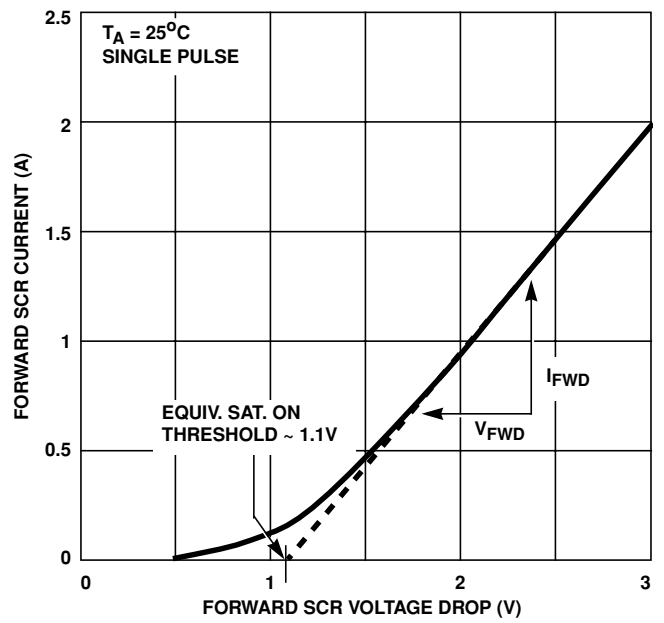


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

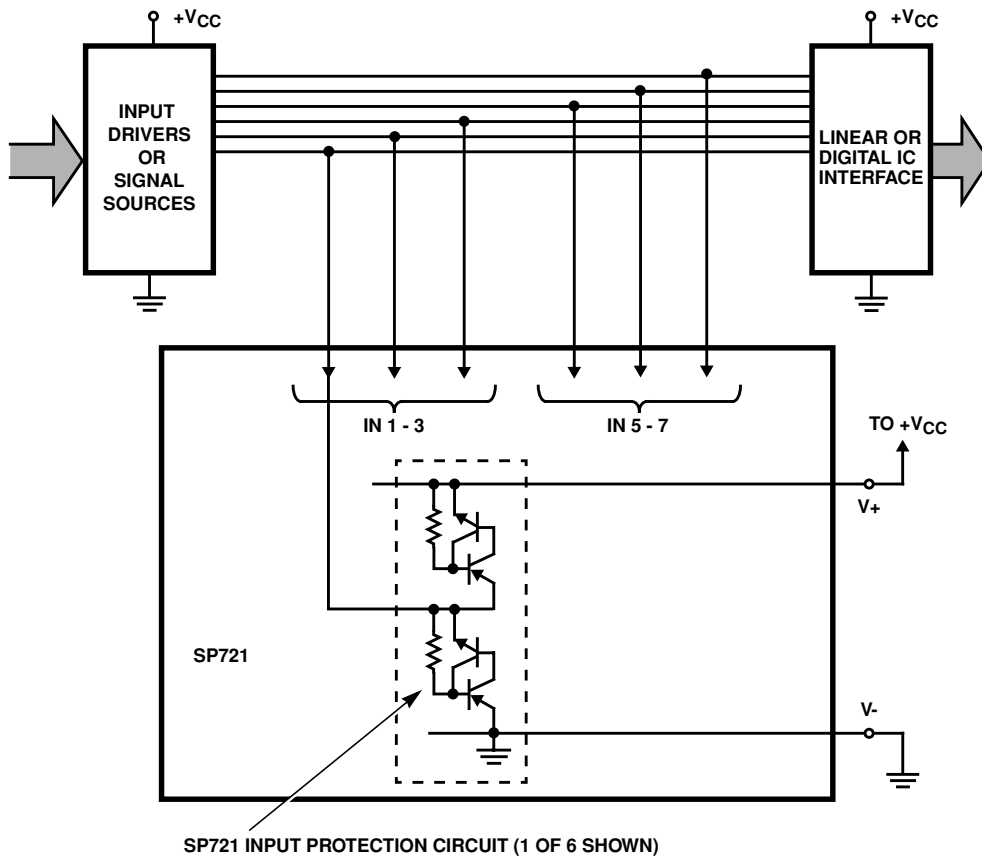


FIGURE 4. TYPICAL APPLICATION OF THE SP721 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE $V+$ OR LESS THAN $-1V_{BE}$ BELOW $V-$

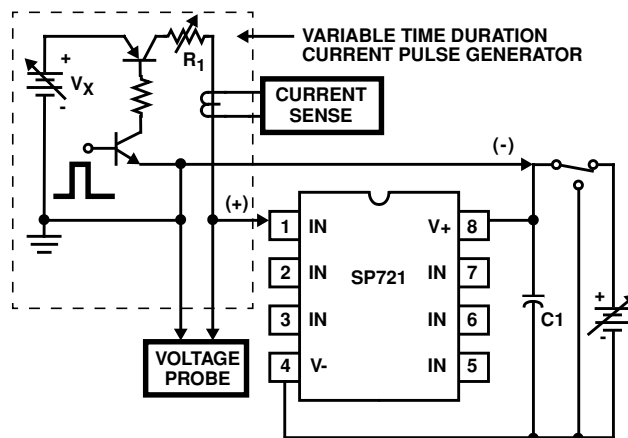
Peak Transient Current Capability of the SP721

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP721's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP721 'IN' input pin and the (+) current pulse input goes to the SP721 V- pin. The V+ to V- supply of the SP721 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25°C and 105°C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP721 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.



$R_1 \sim 10\Omega$ TYPICAL
 V_x ADJ. 10V/A TYPICAL
 $C_1 \sim 100\mu F$

FIGURE 5. TYPICAL SP721 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

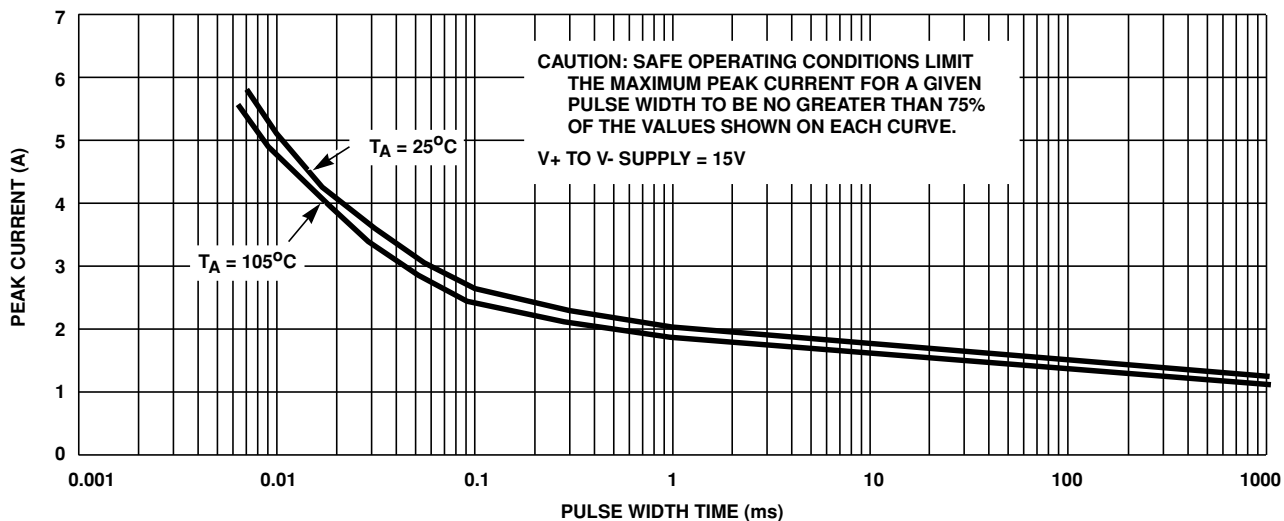
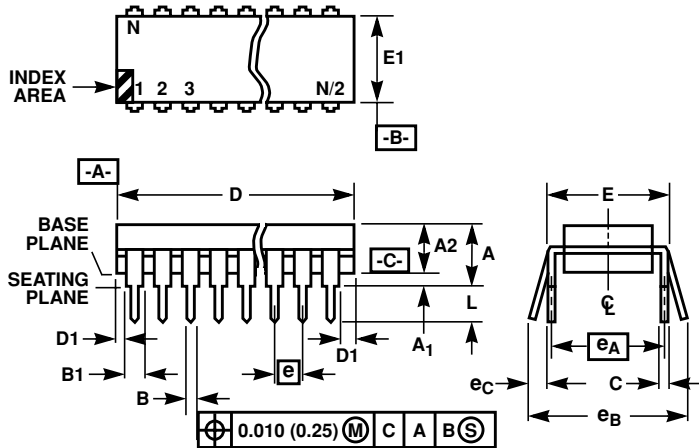


FIGURE 6. SP721 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVERSTRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS

Dual-In-Line Plastic Packages (PDIP)



NOTES:

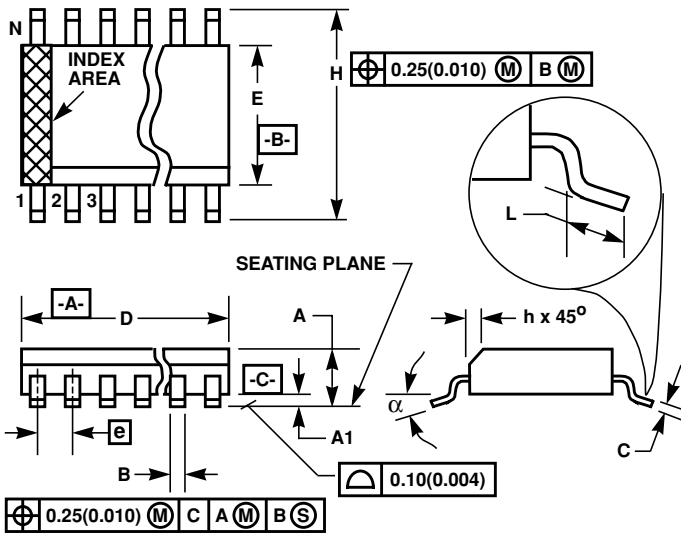
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e _A	0.300 BSC		7.62 BSC		6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



**M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC
PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

All Harris semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Harris semiconductor products are sold by description only. Harris Semiconductor Communications Division reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.

For information regarding Harris' Semiconductor Communications Division and its products, call **1-800-4-HARRIS** or see web site <http://www.semi.harris.com>